



How to Calculate Nanocapacitance

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Abstract: Today, nano-sized capacitors are widely used for storage of electric energy. Consequently, it's too important the knowing how to estimate their capacitance theoretically. This can't be done based on the standard formula useful for macroscopic capacitors with bulk dielectric layers. There is proposed a new formula determining nanocapacitance from effective permittivity and effective thickness of the nanofilm dielectric placed between the nanocapacitor plate-electrodes. This formula explains how the capacitance of a nanocapacitor may significantly differ from its geometric value.

Keywords: Electric Energy Storage, Nanocapacitor, Capacitance, Effective Permittivity, Effective Thickness

1. Introduction

As is known, capacitors play an important role in integrated circuits (ICs): they perform essential functions such as storing electrical charge and blocking direct current while allowing alternating currents to propagate. The highly powered capacitors based on nanostructures are becoming critical for advanced electric energy storage because of their high burst power and storage capability. As ICs continue to be miniaturized, the capacitor must also be miniaturized to realize nanoelectronic circuits.

As a novel device, the nanocapacitor, the dimensions of which are of nanoscale, was presented [1] by considering the effects of material properties on its operation: permittivity, dielectric strength, and quantum-electrical phenomena taking place in metal-insulator-metal (MIM) capacitors on achieving high surface capacitance densities.

The concept of IC nanoelements, including nanocapacitors, was presented and discussed [2] in terms of nanostructures with different from the bulk material properties. Coupled nanoscale circuits and parallel and series combinations were also envisioned, which may provide the technology route for the synthesis of more complex circuits.

Below we describe examples of some constructions proposed so far for nanocapacitors.

High-density arrays of individually isolated semispherical

nanocapacitors, consisting of porous anodic aluminum oxide (AAO) layers as dielectric materials and carbon nanotubes (CNTs) as electrodes, were fabricated [3]. It was shown that the nanocapacitors made with the CNT-electrodes exhibit much better behaviors than those without the CNT-electrodes. The improved electrical behavior was explained in terms of the use of the CNT-electrodes deposited within the porous AAO layers. The capacitance calculated using standard semispherical capacitor formula was found to be in agreement with the experimental value.

A nanocapacitor with ultra-high capacitance (~ 700 pF) was fabricated [4] using electro-deposited gold nanowires manipulated between two gold microelectrodes by the dielectrophoresis technique. A high DC resistance value and nonlinear current-voltage characteristics indicated the formation of a dielectric interface between the nanowires. From frequency dependent conductivity, it was seen that the interface exhibits a giant permittivity: $\sim 2 \cdot 10^7$. The enhancement in permittivity value was attributed to the formation of a disordered interface containing gold atoms disrupted from the surface of the gold nanowires.

The quantum capacitance of a nanocapacitor formed of dielectric-semiconductor (namely, silicon oxide-silicon) layers, deposited alternately with their widths following a Cantor set structure, was calculated numerically [5] and shown that this configuration brings about a nano-hybrid

capacitor which allows both classical and quantum behavior depending on the Cantor generation. In addition, an approximate equivalent circuit representation for the nano-hybrid capacitor was proposed.

MIM electrostatic capacitors fabricated in a 3D cylindrical nanotemplate of anodized AAO porous film have shown profound increase in device capacitance over planar structures. However, inherent asperities at the top of the nanostructure template caused locally high field strengths and led to low breakdown voltage. This severely limits the usable voltage, the associated energy density and thus the operational charge–discharge window of the device. In [6], it was described an electrochemical technique, complementary to the self-assembled template pore formation process in the AAO film, that provides nanoengineered topographies with significantly reduced local electric field concentrations, while reducing leakage current densities by an order of magnitude. In addition, AAO template and nanopore dimensions were optimized to increase the capacitance per planar unit area.

In some cases, the actual capacitance of nanocapacitors is lower than expected from their geometry. A way to mitigate this negative effect was demonstrated [7] by using graded dielectric films instead of homogeneous films. The enhancements were obtained theoretically by using perturbation theory to solve the governing equations with boundary conditions in a model of plate capacitors. It was shown that by grading both the permittivity and the elastic constant, one can obtain a palpable enhancement in capacitance.

In [8], the nickel interdigital capacitors were fabricated on top of silicon substrates. The capacitance of such capacitor was optimized by coating the electrodes with a nanolayer of HfO_2 . An analytical solution of the capacitance equation was compared with results of electromagnetic simulations and measurements. Good agreement between theory and experiments showed that such a modeling would be effective in the design and electrical characterization of nanocapacitors.

It was reported [9] the fabrication process and the electrical characteristics of capacitors with 3D solid state nanocapacitors based on a ZnO nanowire template. Stand-up ZnO nanowires were grown face down on p-type Si substrates coated with a ZnO seed layer. Stacks of $\text{AlZnO}/\text{Al}_2\text{O}_3/\text{AlZnO}$ are then deposited sequentially on the ZnO nanowires using atomic layer deposition. The fabricated capacitor had a high capacitance density (up to $\sim 100 \text{ fF}/\mu\text{m}^2$ at 1 kHz – around 10 times that of the planar capacitor without nanowires) and an extremely low leakage current density. Additionally, the charge–discharge characteristics of the capacitor were investigated and found that the resistance–capacitance time constants were for both the charging and discharging processes were not dependent on the voltage. This reflects good power characteristics of the fabricated capacitors.

Even from this brief review one can conclude that it's too important the knowing how to estimate the nanocapacitance theoretically. However, in general this can't be done based on the standard formula used for macroscopic capacitors with bulk dielectric layers. Present work aims to obtain a formula

useful for calculating nanocapacitances. Proposed expression determines the nanocapacitance via effective permittivity and effective thickness of the nanofilm dielectric placed between the nanocapacitor plate-electrodes.

2. Models

Capacitance C of a thin plate macrocapacitor can be expressed by the formula

$$C = \frac{\epsilon_0 \epsilon S}{d},$$

where ϵ_0 is the electric constant, ϵ is the permittivity of a dielectric layer between two conducting parallel plates – capacitor electrodes, S is the area of a plate, and d is the distance between them – the thickness of the dielectric layer.

It should be noted that, capacitor is considered as a “thin” if both of linear sizes of its electrodes significantly exceed the distance d . Emphasize that a thin capacitor concentrates almost all the electric-field-lines between the plates, i.e., inside its dielectric layer.

Frequently, above stated standard formula does not work for nanocapacitances.

Of course, explanation can be simply related to the capacitor thickness: if plates' linear sizes also are of nanoscale and comparable with d . For “thick” nanocapacitors, it can be recommended an approach similar to calculations performed by us [10] to obtain the nanoparticles near-surface field.

But, there are several quantum effects that can serve for essential reasons of the above mentioned failure. They appear as if two layers of different (from bulk dielectric material) permittivity with capacitances of C_{quantum} are present at the metal/dielectric interfaces and are connected in series with the dielectric film capacitance C , causing a change in the overall capacitance – so-called nanocapacitance C_{nano} :

$$\frac{1}{C_{\text{nano}}} = \frac{1}{C} + \frac{2}{C_{\text{quantum}}}$$

A factor inducing C_{quantum} can be of “geometric” origin. The point is that, when in the nanocapacitor the distances between surfaces of electrode-plates and dielectric layer are comparable with its thickness, the nanothickness d_{nano} is lesser than the distance d between conducting plates: $d_{\text{nano}} < d$. Effect of pair of vacuum “dead-layers” with sum thickness of $d - d_{\text{nano}}$ and very low permittivity ($\epsilon \approx 1$) contradicts the standard formula for macrocapacitance, which suggests that decreasing thickness of a dielectric film should yield increasing capacitance.

In this case, quantum capacitance is positive, $C_{\text{quantum}} > 0$, and consequently reduces C_{nano} . The capacitance reduction at small sizes at the first time was theorized [11] as to be originated from the 2D electron gas accumulated at the atomically thin interface (“dead layer”) between insulator and

a metallic electrode. Further studies have identified two main mechanisms for the “dead-layer” effect: flexoelectricity and incomplete screening. Flexoelectricity refers to the behavior of centrosymmetric, non-piezoelectric dielectrics that if subjected to non-uniform strain can exhibit polarization. As for the incomplete screening, it refers to the phenomenon, where the electric field penetrates into the metal.

On the other hand, the electric properties of a dielectric nanofilm consisting of only a few of atomic layers can't be characterized by the bulk material permittivity ϵ . Instead, one should introduce an effective nanopermittivity ϵ_{nano} , $\epsilon_{\text{nano}} \neq \epsilon$. For example, first-principles quantum-mechanical studies predicted [12] that an ultrathin nanocapacitor made of grapheme (g-C) electrodes and hexagonal boron nitride (h-BN) dielectric nanofilm can achieve superior capacitor properties. The thinnest possible g-C-h-BN-g-C nanocapacitor system was actually fabricated and experimentally demonstrated a significant increase in capacitance below a thickness of $d \approx 5$ nm, more than 100 % of what is predicted by classical electrostatics.

The observed anomalous increase in capacitance with decreasing size suggests that for this particular system the quantum capacitance is negative, $C_{\text{quantum}} < 0$. This effect arises from many-body interactions because the chemical potential of the electrons decreases with the electron density. Near the thin interface layers, the accumulated electron density overscreens the external fields, thus causing an effect opposite to those of the “dead layers”.

Let's note that any of nanostructured materials contains spontaneously formed parasitic capacitors related to existing interfaces of nano-scale thickness and with huge total area. In certain conditions, these built-in capacitors can palpably affect electronic properties of a nanocomposite material. The problem, how to estimate their electric capacitance, will be concerned by us elsewhere [13].

Here, we are focused on nano-sized electrical capacitors that are intentionally formed and used in nanoelectronics for storage of electric charge or energy.

3. Results

The Figs. 1 and 2, respectively, show a normal section of a thin nanocapacitor and corresponding electric field potential distribution. Here the field-lines are parallel to the axis Oz .

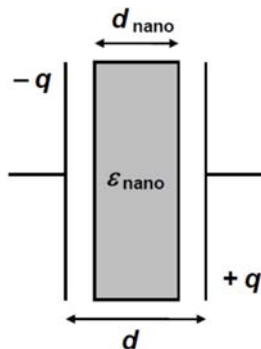


Figure 1. Schematic view of nanocapacitor

Let's denote by q the absolute value of a charge concentrated on a capacitor plate-electrode. It means that, a plate is charged with surface-density of

$$\sigma = \frac{q}{S}.$$

According to the Gauss theorem, within vacuum-layers $-d/2 < z < -d_{\text{nano}}/2$ and $+d_{\text{nano}}/2 < z < +d/2$ absolute value of the electric field strength equals to

$$E = \frac{\sigma}{\epsilon_0} = \frac{q}{\epsilon_0 S},$$

while within the dielectric-layer $-d_{\text{nano}}/2 < z < +d_{\text{nano}}/2$ electric field strength equals to

$$E_{\text{nano}} = \frac{E}{\epsilon_{\text{nano}}} = \frac{q}{\epsilon_0 \epsilon_{\text{nano}} S}.$$

Then, potential drops on vacuum- and dielectric-layers of thickness of $d - d_{\text{nano}}$ and d_{nano} , respectively, are

$$\Delta\phi = E(d - d_{\text{nano}}) = \frac{q(d - d_{\text{nano}})}{\epsilon_0 S}$$

and

$$\Delta\phi_{\text{nano}} = E_{\text{nano}} d_{\text{nano}} = \frac{q d_{\text{nano}}}{\epsilon_0 \epsilon_{\text{nano}} S}.$$

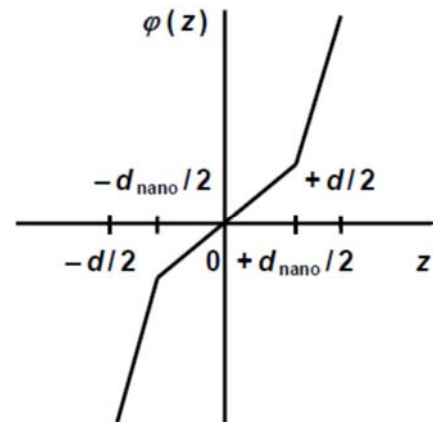


Figure 2. Electric field potential distribution in nanocapacitor

Now we can find voltage applied to the nanocapacitor:

$$U = \Delta\phi + \Delta\phi_{\text{nano}}$$

$$= \frac{qd}{\epsilon_0 S} \left(1 - \left(1 - \frac{1}{\epsilon_{\text{nano}}} \right) \frac{d_{\text{nano}}}{d} \right)$$

and then its capacitance

$$C_{\text{nano}} = \frac{q}{U}$$

$$= \frac{C_0}{1 - \left(1 - \frac{1}{\epsilon_{\text{nano}}} \right) \frac{d_{\text{nano}}}{d}},$$

where

$$C_0 = \frac{\epsilon_0 S}{d}$$

is the capacitance of a thin capacitor of the same geometry, but with vacuum ($\epsilon = 1$) instead of dielectric media between its electrodes.

4. Discussion

It is obvious that, for any dielectric nanolayer effective permittivity should exceed 1, $\epsilon_{\text{nano}} > 1$. On the other hand, its thickness does not exceed distance between plate-electrodes, $d_{\text{nano}} \leq d$. Consequently, the obtained formula yields that $C_{\text{nano}} \geq C_0$. Capacitance reaches its lower limit C_0 when nanocapacitor does not contain any dielectric layer, $d_{\text{nano}} = 0$.

In another limit case, when d_{nano} and ϵ_{nano} tend to d and ϵ , respectively, capacitance tends to C . But, this fact does not mean that anyway macroscopic capacitance C corresponds to the upper limit for the nanocapacitance C_{nano} .

Maximal nanocapacitance, which can significantly exceed macroscopic capacitance, depends on ratios d_{nano}/d and $\epsilon_{\text{nano}}/\epsilon$.

5. Conclusions

In summary, we conclude that capacitance C_{nano} of nano-scale capacitors, which are widely used in nanoelectronics for energy storage purpose, may significantly differ from the capacitance C calculated on basis of standard formula useful for macro-scale capacitors.

There are at least two reasons for this: both effective permittivity ϵ_{nano} and effective thickness d_{nano} of the nano capacitors dielectric layer differ from those, ϵ and d , of bulk dielectric.

Taking into account these factors, we have obtained a

formula determining C_{nano} via ϵ_{nano} and d_{nano} and demonstrated that C_{nano} can significantly differ from C depending on the ratios d_{nano}/d and $\epsilon_{\text{nano}}/\epsilon$.

References

- [1] S.R. Ekanayake, M. Ford, and M. Cortie, "Metal-insulator-metal (MIM) nanocapacitors and effects of material properties on their operation," *Mater. Forum*, vol. 27, pp. 15–20, 2004.
- [2] N. Engheta, A. Salandrino, and A. Alu, "Circuit elements at optical frequencies: Nanoinductors, nanocapacitors, and nanoresistors," *Phys. Rev. Lett.*, vol. 95, pp. 095504, 2005.
- [3] J.I. Sohn, Y.-S. Kim, Ch. Nam, B.K. Cho, T.-Y. Seong, and S. Lee, "Fabrication of high-density arrays of individually isolated nanocapacitors using anodic aluminum oxide templates and carbonnanotubes," *Appl. Phys. Lett.*, vol. 87, pp. 123115, 2005.
- [4] S.K. Saha, M. Da Silva, Q. Hang, T. Sands, and D.B. Janes, "A nanocapacitor with giant dielectric permittivity," *Nanotechnol.*, vol. 17, pp. 2284–2288, 2006.
- [5] R. Montelongo, D. González, R. Bustos, and G. González, "Nanocapacitor with a Cantor multi-layered structure," *J. Mod. Phys.*, vol. 3, pp. 1013–1017, 2012.
- [6] L.C. Haspert, S.B. Lee, and G.W. Rubloff, "Nanoengineering strategies for metal-insulator-metal electrostatic nanocapacitors," *ACS Nano*, vol. 6, pp. 352836, 2012.
- [7] Q. Li, Ch. Patel, and H. Ardebili, "Mitigating the dead-layer effect in nanocapacitors using graded dielectric films," *Int. J. Smart & Nano Mater.*, vol. 3, pp. 23–32, 2012.
- [8] G. González, E.S. Kolosovs–Machuca, E. López–Luna, H. Hernández–Arriaga, and F.J. González, "Design and fabrication of interdigital nanocapacitors coated with HfO_2 ," *Sensors*, vol. 15, pp. 1998–2005, 2015.
- [9] L. Wei, Q.-X. Liu, B. Zhu, W.-J. Liu, Sh.-J. Ding, H.-L. Lu, A. Jiang, and D.W. Zhang, "Low-cost and high-productivity three-dimensional nanocapacitors based on stand-up ZnO nanowires for energy storage," *Nanoscale Res. Lett.*, vol. 11, pp. 213, 2016.
- [10] L. Chkhartishvili, "Nanoparticles near-surface electric field," *Nanoscale Res. Lett.*, vol. 11, pp. 48, 2016.
- [11] M. Stengel and N.A. Spaldin, "Origin of the dielectric dead layer in nanoscale capacitors," *Nature*, vol. 443, pp. 679–682, 2006.
- [12] G. Shi, Y. Hanlunmyuang, Zh. Liu, Y. Gong, W. Gao, B. Li, J. Kono, J. Lou, R. Vajtai, P. Sharma, and P.M. Ajayan, "Boron nitride-grapheme nanocapacitor and theorizing of anomalous size-dependent increase of capacitance," *Nano Lett.*, vol. 14, pp. 1739–1744, 2014.
- [13] L. Chkhartishvili, A. Gachechiladze, O. Tsagareishvili, and D. Gabunia, "Capacitances built in nanostructures," in *Proc.18th Int. Metall. Mater. Cong.*, 2016 – in press.